1359662

PATENT SPECIFICATION

(11) 1359662

(21) Application No. 35534/71 (22) Filed 28 July 1971
(31) Convention Application No. 76787 (32) Filed 30 Sept. 1970 in
(33) United States of America (US)
(44) Complete Specification published 10 July 1974
(51) International Classification G06F 3/04
(52) Index at acceptance
G4A 11B 19 3W2 5B 6N 6M1
H4P B2 B6A B6B B6C B6Y E1 E7

(19)

(54) IMPROVEMENTS IN OR RELATING TO DATA COMMUNICATION SYSTEMS

(71) We, HONEYWELL INFORMATION SYSTEMS INC. a Corporation organised and existing under the laws of the State of Delaware, United States of America of 200 Smith Street, Waltham, Massachusetts, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed to be particularly described in and by the following statement:—

The present invention pertains to data communications systems and more specifically to a data communications controller which can be used to scan all of the subchannels connected thereto when a priority switch is open. When the priority switch is closed a selector switch on the communications controller can be used to choose one of several combinations of subchannels which are awarded priority over other subchannels being scanned.

Electronic data processing has rapidly become a necessary adjunct to everyday business and provides not only means for calculating, accounting and general data processing, but also provides a source of business management information. To incorporate a data processing system into a business frequently requires transmission into the system over long distances. Terminal devices convert data from human readable form into binary form and transmit this data over wires or microwave relay systems from the terminal device to the data processor. The data processor operates upon the data received and sends a return message to the terminal device. The data processor operates at a speed which is many times as fast as the operating speed of the terminal devices. To provide efficient use of the data communications equipment a control module such as a communications controller is connected between the terminal devices and the data processor. These terminal devices generate a wide variety of message code sets, character lengths and bit rates. The data is transmitted a bit at a time from the terminal devices to the subchannels which temporarily store the data and then send the data to the processor. The rate of transmission of the data from the terminal device is much slower than the operating speed of the data processor so that there is a considerable period of time between the receipt of the first data bit from terminal number one and the receipt of a second data bit from this same terminal. This means that the communications controller can receive a first data bit from terminal device number 1, then receive a data bit from terminal device number 2, etc. and return back to terminal number 1 in time to receive the second data bit from terminal device number 1. The communications controller is designed so that it continuously scans through all of the subchannels connected to the communications controller and receives one bit at a time from each of these subchannels. However, if some of the terminal devices provide data bits at a higher rate it may be advantageous to receive more than one data bit from a high speed terminal device before proceeding to one of the lower speed terminal devices. Therefore, it is desirable that a priority system be used such that the higher speed devices receive a higher priority and be scanned several times while the lower speed devices are scanned or are connected to the controller only a single time. It is therefore advantageous to develop a communications controller having a dual scanning system so that all of the subchannels connected to the controller can be scanned in order when there is no high speed terminal device connected to the subchannel, but to assign priority to a terminal device having a higher speed when it is connected to the controller.

It is, therefore, an object of this invention to provide a communications controller having a dual scanning system.

According to the present invention, there is provided a digital electric data communications system incorporating a priority switch and a data communications controller for controlling the sequential polling of a plurality of subchannels, said controller comprising a pair of subchannel scanners one of which is

arranged to generate signals when activated which cause the sequential polling of all the said subchannels and the other is arranged to generate signals when activated which cause the sequential polling of some, but not others, of said subchannels, and a priority selection circuit which enables one or other of the said scanners in accordance with the setting of the priority switch and the presence or absence of a demand for priority servicing from one or more of the subchannels polled by the second said subchannel scanner, said first scanner thus being enabled in the absence of said priority demand signals and, subject to the setting of the said priority switch, being disabled upon manifestation of said signals.

The first said subchannel scanner scans each of the subchannels in turn. The second said subchannel scanner is used to scan the priority subchannels when any of these priority subchannels request such action. When no priority requests are received the communication controller returns to the normal scanning.

In an embodiment of the invention described herein there is provided a data communication system having dual scanners for use with a plurality of subchannels, said system comprising: first and second counters; an oscillator, said oscilator being connected to said first and said second counters; means for disabing said counters; first and second switching means, said first switching means being connected between said first counter and said means for disabling, said first switching means being connected to said second counter, said first switching means selectively connecting one of said first and said second counters to said means for disabling; and a decoding matrix, said second switching means being connected between said matrix and said first counter, said second switching means being connected to said second counter, said second switching selectively connecting one of said first and said second counters to said matrix, said matrix being coupled to said subchannels.

Arrangements in accordance with the invention will now be described by way of example and with reference to the accompanying drawings, in which: —

Figure 1 is a simplified block diagram of a data communications system in which the present invention may be used.

Figs. 2a and 2b are a simplified schematic diagrams of a typical subchannel constructed in accordance with one embodiment of the present invention.

Figs. 3a—d are simplified schematic diagrams of a data communications controller constructed in accordance with this embodiment.

Fig. 4 illustrates waveforms which are useful in explaining the operation of the embodiment shown in Figs. 2 and 3.

Fig. 5 illustrates the various methods of scanning which may be employed by the communications controller shown in Fig. 3.

Fig. 6 comprises a schematic diagram showing details of the channel enable decoding matrix of Fig. 3.

Fig. 7 shows another embodiment of the high priority scanner of Fig. 3.

Description of the Preferred Embodiment

The data communication system shown in Fig. 1 includes a data processor 1, a memory controller 2, a memory 3, an input/output multiplexer 4, a communications controller 5, and a plurality of subchannels 6a—6n. The data processor manipulates data in accordance with instructions of a program. The processor receives an instruction, decodes the instruction and performs the operation indicated thereby. The operation is performed on data received by the processor and temporarily stored thereby during the operation. The series of instructions are called a program and include decodable operations to be performed by the processor. The instructions of the program are obtained sequentially by the processor and together with the data to be operated upon, are stored in the memory. The memory 3 shown in Fig. 1 may form many of several well known types; however, most commonly, the main memory is a random access conicident current type having a plurality of addressable locations each of which provides storage for a word. The word may form data or instructions and may contain specific fields useful in a variety of operations. Normally, when the processor is in need of data or instructions it will generate a memory cycle and provide an address to the memory. The data or word stored in the address location will subsequently be retrieved from memory and provided to the data processor 1.

A series of instructions comprising a program are usually "loaded" into the memory at the beginning of the operation and thus occupy a "block" of memory which normally must not be disturbed until the program has been completed. Data to be operated upon by the processor in accordance with instruction of the stored program is stored in memory and is retrieved and replaced in accordance with the binary coded instructions.

Communication with the data processing system usually takes place through the media of input/output devices such as magnetic tape handlers, paper tape readers, punched card readers, and remote terminal devices. To control the receipt of information from the input/output devices and to coordinate the transfer of information to and from such devices, an input/output control means is required. Thus, an input/output controller or input/output multiplexer is provided and connects the data processing system to the variety of input/output devices. The input/output multiplexer coordinates the information flow to and from the

various input/output devices and also awards priority when more than one input/output device is attempting to communicate. Since input/output devices are usually electro-mechanical in nature and necessarily have operating speeds which are much lower than the remainder of the data processing system, the input/output multiplexer provides buffering or temporary storage to enable the processing system to proceed at its normal rate without waiting for the time consuming communication with the input/output device.

The input/output multiplexer shown in Fig. 1 may have a plurality of input/output devices connected to the input/output multiplexer or the input/output controller in the same manner as Fig. 1 of U.S. Patent No. 3,413,613. The communications controller 5 appears to the input/output multiplexer 4 to be an input/output device, but this communications controller in turn controls a plurality of subchannels which may be connected through modems and telephone lines to terminal devices.

Binary information which may be supplied from the memory to the subchannel 6a—6n, is converted by one of the local modems 8a—8n into a modulated signal which may be sent over telephone lines 9a—9n to one of the terminal modems 10a—10n. A terminal modem converts a modulated signal into binary information for use by corresponding one of the terminal devices 11a—11n. Binary information which is generated by one of the terminal devices 11a—11n is converted by one of the terminal modems 10a—10n into a modulated signal which is sent over the telephone lines to a corresponding local modem 8a—8n, which converts the signal into binary information again for use by a corresponding one of the subchannels 6a—6n. The local modems and the terminal modems may either receive modulated signals and convert the modulated signals into binary information or they may receive binary information and convert it into modulated signals.

For a complete description of the processor of Fig. 1 reference is made to the above mentioned U.S. Patent No. 3,413,613. More particularly, Figs. 10—38 of the drawings; column 10, line 67 to column 32, line 21 of U.S. Patent No. 3,413,613 are incorporated herein by reference and are made a part of the present specification.

Memory device 3 may be of the type disclosed in U.S. Patent No. 3,521,240.

A more complete description of the operation of a data communication system is disclosed in copending British patent application No. 11454/71 (Serial No. 1352055). A portion of one of the subchannels 6a—6n is shown in more detail in Fig. 2 and a portion of the communications controller 5 is shown in Fig. 3. The communications controller of Fig. 3 (Fig. 3a, 3b, 3c) includes a high priority scanner 84, a normal scanner 88 and a channel enable decoding matrix 94 which supplies channel enable signals to the subchannels 6a—6n. The controller of Fig. 3 scans each of the subchannels in turn by sequentially providing an enable signal to each of the subchannels. The controller has a plurality of priority switches to enable the controller to scan only a predetermined number of high priority subchannels when a predetermined number of these priority switches are closed. When all of the priority switches are open, the controller sequentially provides enable signals to each of the subchannels 6a—6n of Fig. 1.

The controller shown in Fig. 3 is designed to scan 32 subchannels with the normal scanner and to scan either 2, 4, 8 or 16 subchannels as high priority subchannels when priority switches in the controller are closed and priority signals are received from the subchannels. It should be understood that the controller in Fig. 3 can be changed to scan a greater or lesser number of subchannels by changing the number of elements in the scanners.

AND-gates

The AND-gates disclosed in the drawings and particularly in Figs. 2 and 3 provide the logical operation of conjunction of binary signals applied thereto. In the system disclosed, since the binary 1 is represented by a positive signal, the AND-gates provide the positive output signal representing a binary 1 when, and only when all of the input signals applied thereto are positive and represent binary 1's. The symbols identified by the numerals 51—54 in Fig. 2 represent two-input AND-gates. Such AND-gates deliver a binary 1 output signal only when each of the two-input signals applied thereto represents a binary 1. A three-input AND-gate, such as represented by AND-gate 55, delivers a binary 1 output only when each of the three-input signals represent a binary 1.

OR-gate

The OR-gates disclosed in Fig. 2 and 3 provide logical operation of inclusive-OR function for binary 1 input signals applied thereto. In the system, since the binary 1 is represented by positive signals, each OR-gate provides a positive output signal representing a binary 1 when any one or more of the input signals applied thereto is positive and represent binary 1's. The symbol identified by gate 31 in Fig. 2 represents a three-input OR-gate. This OR-gate delivers a binary 1 output signal when any one or more of its input signals applied thereto represents a binary 1.

Inverter

The inverter disclosed in Fig. 2a and represented by numerals 14, 28, etc. provides a positive output signal representing a binary

1 when the input signal applied thereto is negative, representing a binary 0. Conversely, the inverter provides an output signal representing a binary 0 when the input signal represents a binary 1.

Flip-Flop

The flip-flops or bistable multivibrators referred to in the specification, and shown, for example, in Fig. 3 of the drawings, are circuits adapted to operate in either one of two stable states and to transfer from the state in which they are operating to the other stable state upon the application of a trigger signal thereto. In one state of operation, the flip-flop represents the binary 1 (1-state) and in the other state the binary 0 (0-state). The three leads entering the left-hand side of the flip-flop symbol, for example, flip-flop number 75, shown in Fig. 3a, provide the required trigger signals. The upper lead, the J lead, provides the set signal, the lower lead, the K lead, provides the reset input signal and the center lead provides the trigger signal. When this set input signal, on the J lead, is positive and the reset signal, on the K lead is zero, a change from a positive voltage to a zero value of voltage, on the C lead, cause the flip-flop to transfer to its 1-state, if it is not already in the 1-state. When the reset signal is positive and the set signal is zero, a change from a positive voltage to a zero value of voltage, on the C lead, causes the flip-flop to transfer to the 0-state if it is not already in the 0-state.

When the J and K input leads are both positive, or when the J and K leads are not connected to an external signal source, a positive trigger pulse causes the flip-flop to change states. The R lead entering the bottom of the flip-flop also provides reset signals. When a zero voltage potential is applied to the R lead, the flip-flop resets to the 0-state and remains in the 0-state as long as the zero voltage potential remains on the R lead, irrespective of any signals on the J, C and K leads. Some flip-flops do not provide the R lead. The two leads leaving the right-hand side of the flip-flops deliver the output signal for each flip-flop. The upper output leads, the Q leads, deliver the 1-output signal of the flip-flop and the $\overline{Q}$ output leads, deliver the 0-output signals.

Scanner

The operation of the scanners used in the controller can be more clearly seen by referring to the normal scanner or counter 88 in Fig. 3. Pulses from the oscillator 90 are coupled to the input of the normal scanner 88 which comprises a plurality of flip-flops 89a—89e. When a positive voltage from AND-gate 87 is applied to the J and K input of flip-flop 89a, each of the trigger pulses applied to the C input causes flip-flop 89a to change states. When two pulses have been received at the input of flip-flop 89a, a positive output voltage is produced at the Q output lead of flip-flop 89b and is applied to one lead of AND-gate 91b. When eight pulses have been received at the input lead of flip-flop 89a, a positive voltage is applied from the Q output lead of flip-flop 89d to the C lead of flip-flop 89e and to one lead of AND-gate 91d. When twelve pulses have been received a positive voltage from both the Q output lead of flip-flop 89e and the Q output lead of 89d is applied to the input leads of AND-gates 91c and 91d. When a positive voltage from flip-flop 81 is applied to the other leads of AND-gates 91c and 91d the positive signals from scanner 88 are coupled through OR-gates 92c and 92d to provide a positive signal on each of the leads CN4 and CN8. A more complete discussion of the binary scanner or binary counter shown in Fig. 3 can be found in the textbook "Digital Computer Fundamentals", second edition, by Thomas C. Bartee, McGraw Hill, 1966 on pages 94—96.

Signals from the Q output leads of flip-flops 89a—89e of the scanner 88 are coupled through AND-gates 91a—91e and OR-gates 92a—92d to the leads CN1—CN16 which are coupled to the channel enable decoding matrix 94. The channel enable decoder matrix 94 is shown in more detail in Fig. 6. The signals from the leads CN1—CN16 are selectively coupled to the AND-gates 98a—98n and are applied to the inverters 99a—99e. Inverters 99a—99e invert the signals which are also selectively coupled to AND-gates 98a—98n. For example, the inverted signals are applied to the input leads of AND-gate 98a so that a positive signal is developed at the output of AND-gate 98a when the count in the counter or scanner 88 is equal to zero. This positive signal provides an enable signal to subchannel 0 shown in Fig. 1. When the first pulse is applied to the trigger lead of flip-flop 89a in the scanner 88, a positive signal is applied on the CN1 output lead, thereby providing a positive signal to the upper lead of AND-gate 98b. All of the other leads CN2—CN16 have a signal representing a binary zero which is inverted by inverters 99b—99e respectively and applied to the other lead of AND-gate 98b causing gate 98b to provide a positive signal at the output lead of AND-gate 98b thereby providing a positive enable signal to channel 1. As the count in the scanner 88 proceeds, the leads from the flip-flops 89a—89e provide positive signals which sequentially enable the other gates 98a—98n to sequentially provide an enable signal to each of the other subchannels of the system shown in Fig. 1. These enable signals are coupled to the subchannels on input leads 33 shown in Figs. 2 and 3.

The operation of the communications controller 5 will now be described in connection

with Figs. 2, 3, 4, 5 and 6. Fig. 2 shows a typical subchannel which may be connected between the local modem and the communications controller shown in Fig. 1. The subchannel shown in Fig. 2 communicates with the modem over the lines shown on the left-hand side of the Fig. 2a and communicates with the communications controller over the lines shown on the right-hand side of Fig. 2b. Figs. 2a and 2b are drawn to be placed side by side so that the leads from the right side of Fig. 2a are connected to the leads from the left side of Fig. 2b. The subchannel receives input data, timing signals and carrier detect signal from the modem and sends output data to the modem over line 19. The subchannel receives channel-enable signals, answer signals and output data from the controller over lines shown at the right-hand side of the sheet and supplies input data and a plurality of commands to the communications controller over other lines shown at the right-hand side of the Fig. 2b.

When the modem is in operation, timing signals are continuously supplied to the subchannel over input lines 17 and 23 and input data is supplied over line 13. When a binary bit of data is applied to line 13, this binary bit and the timing signal on line 17 cause the binary bit to be set into input-data flip-flop 15 and the timing signal also sets the bit-ready flip-flop 16. When the bit-ready flip-flop 16 is set a binary one which is developed at the Q output lead is transferred through OR-gate 31 to one lead of AND-gate 35. When the channel-enable signal from the communications controller is supplied to the particular channel over line 33, gate 35 is enabled so that a service-request signal is supplied to the communications controller. The binary 1 from the Q output lead of flip-flop 16 also sets the store-command flip-flop 46. At this same time, the channel enable signal enables AND-gate 34 so that the binary bit which was stored in input-data flip-flop 15 is gated through gate 34 to line 38 which provides input data to the communications controller. The service-request signal is applied to OR-gate 96a in the communications controller shown in Fig. 3c and is coupled to the J input lead of the scan flip-flop 75 in Fig. 3a. Figs. 3a, 3b and 3c are drawn to be placed side by side as shown in Fig. 3d. Leads from the right side of Fig. 2a are connected to the leads from the left side of Fig. 2b. Leads from the right side of Fig. 2b are connected to the leads from the left side of Fig. 2c.

The service-request signal on the J lead of scan flip-flop 75 and the oscillator pulse which is delayed by delay line 74 and applied to the C input lead cause the flip-flop 75 to be set and to provide a binary 1 at the Q output lead. The binary 1 from the Q output lead of flip-flop 75 provides an interrupt signal to the input/output multiplexer, Fig. 1, which provides an answer signal when the input/output multiplexer has accepted the data. This answer signal which is provided on line 45 is coupled to line 45 of the subchannel and is applied to one lead of AND-gate 36. The channel-enable signal from line 33 is applied to a second lead of AND-gate 36. The binary 1 from the Q output lead of bit-ready flip-flop 16 has previously set the store command flip-flop 46 so that flip-flop 46 provides a binary 1 at its Q output and supplies a third binary 1 to the input of AND-gate 36. These binary 1's cause the answer signal from the controller to be gated through the inverter 28 and to provide a reset signal to bit ready flip-flop 16. The answer signal also provides a pulse to inverter 76 which inverts the pulse and causes scan flip-flop 75 to be reset, thereby providing a binary 1 at the $\overline{Q}$ output lead of flip-flop 75.

The binary 1 at the $\overline{Q}$ output lead of flip-flop 75 enables AND-gates 83 and 87 so that signals from scanner-select flip-flop 81 are coupled to the J and K input leads of either flip-flop 85a in the high priority scanner 84 or are coupled to flip-flop 89a in normal scanner 88. These signals from the scanner-select flip-flop select either the high priority scanner or the normal scanner to provide scanning signals to the channel enable decoding matrix 94.

When it is desired that the normal scanner be used on all subchannels the switch 30 (Fig. 2) in each subchannel is open so that a low value of voltage representing a binary 0 is coupled on line 39 to the communications controller of Fig. 3. This binary 0 is coupled through OR-gate 96b and inverted by inverter 77 causing scanner-select flip-flop 81 to be reset and to provide a binary 1 at the $\overline{Q}$ output lead. The binary 1 at the $\overline{Q}$ output lead enables AND-gates 91a—91e and AND-gate 87 so that the normal scanner 88 provides signals to the channel enable decoding matrix 94.

When the modem is ready to receive data from the subchannel, timing signals are provided over line 23 to the bit-request flip-flop 25 thereby setting flip-flop 25. When the bit-request flip-flop 25 is set a binary 1 from the Q output lead is coupled through OR-gate 31 and AND-gate 35 to the communications controller. At this time if the bit-ready flip-flop 16 is reset the binary 0 from the Q output lead is inverted by inverter 43 and applied to one lead on the AND-gate 54 of Fig. 2b. The binary 1 from the Q output lead of bit-request flip-flop 25 is applied to the other lead of AND-gate 54 thereby causing the load-command flip-flop 47 to be set. The binary 1 from the Q output lead of load-command flip-flop 47 and the answer signal from the

input/output multiplexer on line 45 and the channel-enable signal on line 33 enable AND-gate 37 so that data from the input/output multiplexer on line 49 is gated into the output-data flip-flop 21 (Fig. 2a). When the next timing pulse is received by the subchannel, the data bit in output-data flip-flop 21 is gated into output flip-flop 20 and is coupled over line 19 to the modem.

Whenever a carrier signal from the modem changes, for example, the carrier comes on or the carrier goes off, a voltage is provided over line 63 to the subchannel. When the carrier goes off, a negative going signal is applied to the carrier-off flip-flop 64 thereby setting flip-flop 64. When the carrier comes on a positive going signal on line 63 is inverted by inverter 67 and sets the carrier-on flip-flop 65. Signals from carrier-off flip-flop 64 and carrier-on flip-flop 65 may be coupled through OR-gate 70, OR-gate 31 and AND-gate 35 to provide a service-request signal to the communications controller. The signal from the carrier-off flip-flop is also coupled through AND-gate 62 to the communications controller and the signal from the carrier-on flip-flop 65 is coupled through AND-gate 69 to the communications controller. The data-load signals, the data-store signals, the status-store signals, the carrier-on signals, and the carrier-off signals are coupled through AND-gates 96d—96h (Fig. 3c) to the input/output multiplexer shown in Fig. 1.

When it is desired that the subchannel shown in Fig. 2 be used as a high priority subchannel, the switch 30 is closed. Thus each time that the bit is ready to be transferred from the subchannel to the communications controller, a signal from the Q output lead of the bit-ready flip-flop 16 is applied through OR-gate 29 and switch 30 to the priority request line 39 and to the communications controller. If a bit is ready to be set to the modem the bit-request flip-flop 25 is set so that a binary 1 is available at the Q output lead of flip-flop 25. This binary 1 is coupled through OR-gate 29 and switch 30 to the priority request line 39. The priority-request signal on line 39 (Fig. 3) is coupled through OR-gate 96b to the one input lead of AND-gate 79. The other input lead to AND-gate 79 is enabled by the signal from the $\overline{Q}$ lead of scan flip-flop 75 so that the scanner-select flip-flop 81 is set when the next pulse from oscillator 90 is applied to the C input lead. When flip-flop 81 is set, a binary 1 at the Q output lead enable AND-gates 86a—86d so that the output of the high priority scanner 84 will be coupled to the channel decoding matrix 94 and out to the various subchannels. At this same time a binary 0 from the $\overline{Q}$ output lead disables AND-gate 87 so that the normal scanner 88 is disabled and scanning by scanner 88 is halted.

When it is desired that only two high priority subchannels be used with the communications controller shown in Fig. 3, the switch 82a in Fig. 3b is connected to the contact 78a. Switches 82b, 82c and 82d are each connected to the ground contacts. With the switches in the above position, only the binary bit from the flip-flop 85a is coupled through gate 86a to the channel-enable decoder matrix 94 so that only subchannel 0 and subchannel 1 are scanned by the high priority scanner. When it is desired that more than two subchannels be used as high priority channels, other of the switches 82a—82d are connected to the corresponding contacts 78a—78d. For example, when it is desired that eight subchannels be used as high priority channels, the switches 82a, 82b and 82c are connected to contacts 78a, 78b and 78c respectively. When it is desired that sixteen subchannels be used as high priority channels, all of the switches 82a—82d are connected to their respective contacts 78a—78d. Thus, it can be seen that the high priority scanner shown in Fig. 3 causes the communications controller to scan two channels, four channels, eight channels or sixteen channels as high priority channels. If it is desired that other numbers of channels be scanned such as three or five, another embodiment of the high priority scanner, shown in Fig. 7, can be used. The scanner shown in Fig. 7 can be used to continuously select any number from one channel to sixteen channels for high priority channels. It should be understood that more than sixteen channels can be scanned by including additional flip-flops and additional switches in the circuit shown in Fig. 7.

When all of the high priority subchannels, as shown in Fig. 2, have been serviced, the bit-ready flip-flops 16 and the bit-request flip-flops 25 in each of the subchannels are reset so that there are no longer any signals on the priority request lines 39 from the subchannels to the communications controller. When there is no signal on line 39 there is no signal from OR-gate 96b in the communications controller so that the voltage applied to the input of AND-gate 79 (Fig. 3b) is low and AND-gate 79 is disabled. The low value of voltage is inverted by inverter 77 and applied to one lead of AND-gate 80 so that the binary 1 from the $\overline{Q}$ lead of scan flip-flop 75 is coupled through AND-gate 80 and resets the scanner-select flip-flop 81. When flip-flop 81 is reset, a binary 1 from the $\overline{Q}$ output lead of flip-flop 81 is coupled to one lead of AND-gates 91a—91e so that gates 91a—91e are enabled. The normal scanner 88 is again coupled to the channel enable decoding matrix 94 and all

of the subchannels will be sequentially scanned by the communications controller.

If the normal scanner is providing channel-enable signals to one of the channels 17—31 at the time that a priority-request signal is received from one of the high priority subchannels, normal scanner 88 will stop scanning. However, the communications controller will finish servicing the subchannel which was being serviced at the time the priority-request signal was received. The high priority scanner will start scanning the high priority channels which are determined by the settings of the switches 82a—82d. When the priority-request signal is no longer applied to the communications controller, the normal scanner will resume scanning the channels starting with the next channel which is due to be serviced. For example, if the normal scanner had stopped on subchannel 19 at the time the priority-request signal caused the high priority scanner to start operations, the normal scanner will resume scanning at subchannel 20.

A priority of commands from the subchannel to the controller is established by flip-flops 46, 47, 48, inverters 43, 58, 59, 60 and AND-gates 54 and 55. Only one of the flip-flops 46, 47 and 48 can be set at any given time so that only one of the data-store, data-load and status-store signals can be sent to the communications controller at any given time. The flip-flops 46, 47 and 48 are set by signals from flip-flops 16, 25, 64 and 65.

When bit-ready flip-flop 16 is set a binary 1 from the Q output lead and a service-request signal from AND-gate 35 cause store-command flip-flop 46 to be set and to provide a data-store command to the communications controller. The binary 1 from flip-flop 16 is inverted by inverter 43 and disables AND-gates 54 and 55 so that flip-flops 47 and 48 cannot be set.

When bit-request flip-flop 25 is set and bit-ready flip-flop 16 is reset a binary 0 from the Q output lead of flip-flop 16 is inverted by inverter 43 and applied to one lead of AND-gate 54 thereby enabling AND-gate 54 so that a binary 1 from the Q output lead of flip-flop 25 causes load-command flip-flop 47 to be set and to provide a data-load command to the controller. The binary 1 from flip-flop 25 is inverted by inverter 58 and disables AND-gate 55 so that flip-flop 48 cannot be set.

When flip-flops 16 and 25 are both reset binary 0's from the Q output leads of flip-flops 16 and 25 are inverted by inverters 43 and 58 and applied to AND-gate 55 thereby enabling AND-gate 55 so that a binary 1 from the Q output lead of either carrier-OFF flip-flop 64 or carrier-ON flip-flop 65 causes status-command flip-flop 48 to set. When flip-flop 48 is set a binary 1 from the Q output lead provides a status-store command to the communications controller.

WHAT WE CLAIM IS:—

1. A digital electric data communications system incorporating a priority switch and a data communications controller for controlling the sequential polling of a plurality of subchannels, said controller comprising a pair of subchannel scanners one of which is arranged to generate signals when activated which cause the sequential polling of all the said subchannels and the other is arranged to generate signals when activated which cause the sequential polling of some, but not others, of said subchannels, and a priority selection circuit which enables one or other of the said scanners in accordance with the setting of the priority switch and the presence or absence of a demand for priority servicing from one or more of the subchannels is polled by the second said subchannel scanner, said first scanner thus being enabled in the absence of said priority demand signals and, subject to the setting of the said priority switch, being disabled upon manifestation of said signals.

2. A system according to Claim 1 wherein the subchannel scanners comprise multistage counters and the controller incorporates an oscillator arranged to clock scanning bits through the said counters, the stage outputs of the counters being connected to a decoding matrix via respective gating means which are selectively enabled by the operation of the said priority selection circuit.

3. A system according to Claim 2 wherein the said subchannel scanners each comprise a plurality of flip-flops.

4. A data communications system according to any of Claims 1 to 3 wherein the said second subchannel scanner includes switching means for selecting the number of subchannels to be given priority of service.

5. A system according to Claim 4 when appendant to Claim 2 wherein the said switching means appertaining to the second subchannel scanner is connected between the stage outputs of the second scanner and the corresponding gate inputs of the said respective gating means.

6. A system according to Claim 4 when appendant to Claim 2 wherein the said switching means appertaining to the second scanner comprises selector switches connected so as to select from between the respective Q and $\overline{Q}$ outputs of the second scanner as defined herein, said switching means thereby providing a plurality of conditioning inputs to an AND

gate the output of which is used to reset the counting stages of the second scanner.

7. A digital electrical data communication system substantially as described with reference to Figures 1 to 6 of the accompanying drawings, or as modified according to Figure 7.

For the Applicants:
LLOYD WISE, BOULY & HAIG,
Chartered Patent Agents,
Norman House,
105—109 Strand,
London, WC2R 0AE.

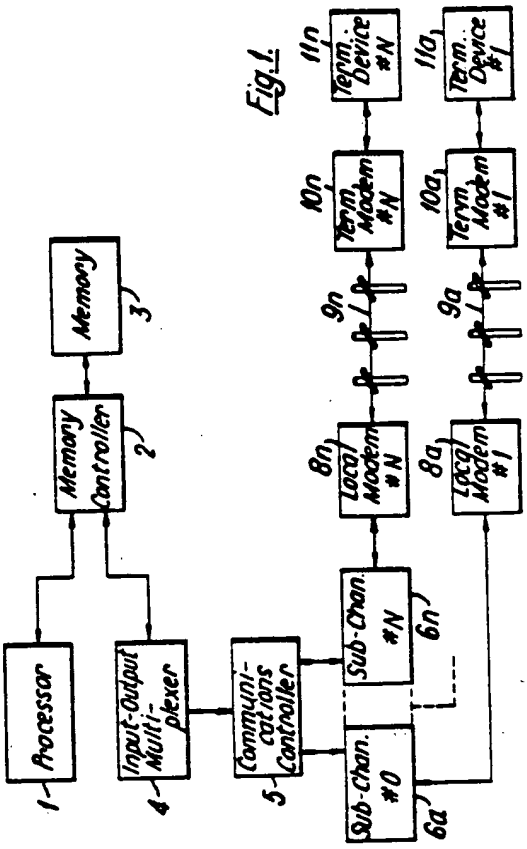
Printed for Her Majesty's Stationery Office, by the Courier Press, Leamington Spa, 1974.
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.

1359662 COMPLETE SPECIFICATION

9 SHEETS This drawing is a reproduction of the Original on a reduced scale

Sheet 1

Fig.1.



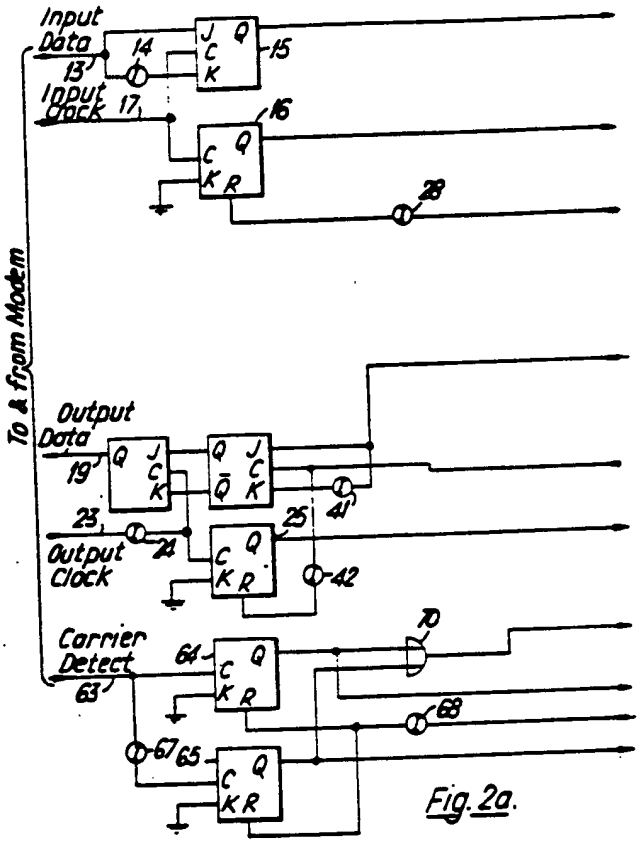

Input Data
13
14
15
Input Clock
17
16
28
To & from Modem
Output Data
19
23
24
25
41
Output Clock
42
Carrier Detect
63
64
70
68
67
65

Fig. 2a.

1359662 COMPLETE SPECIFICATION
9 SHEETS This drawing is a reproduction of the Original on a reduced scale
Sheet 3

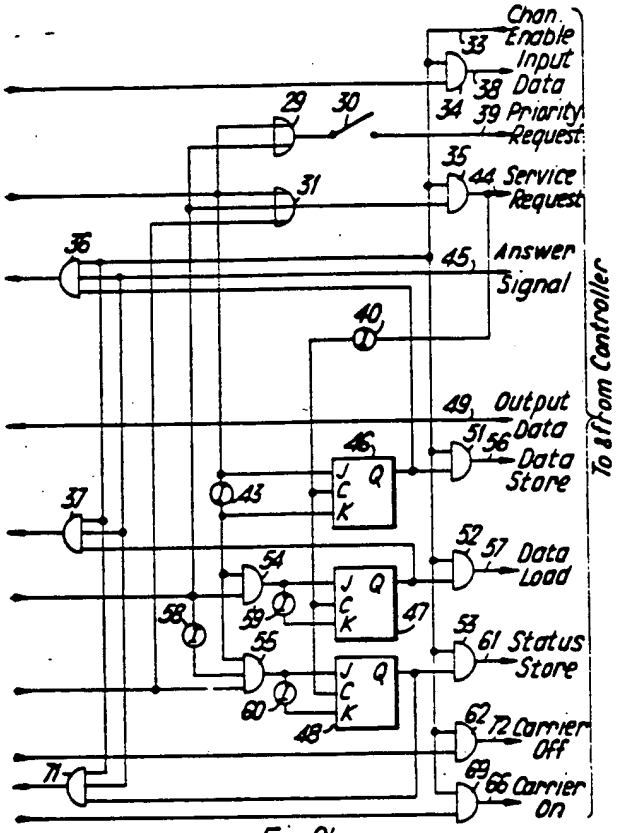


Fig. 2b.

1359662 COMPLETE SPECIFICATION
9 SHEETS This drawing is a reproduction of the Original on a reduced scale
Sheet 4

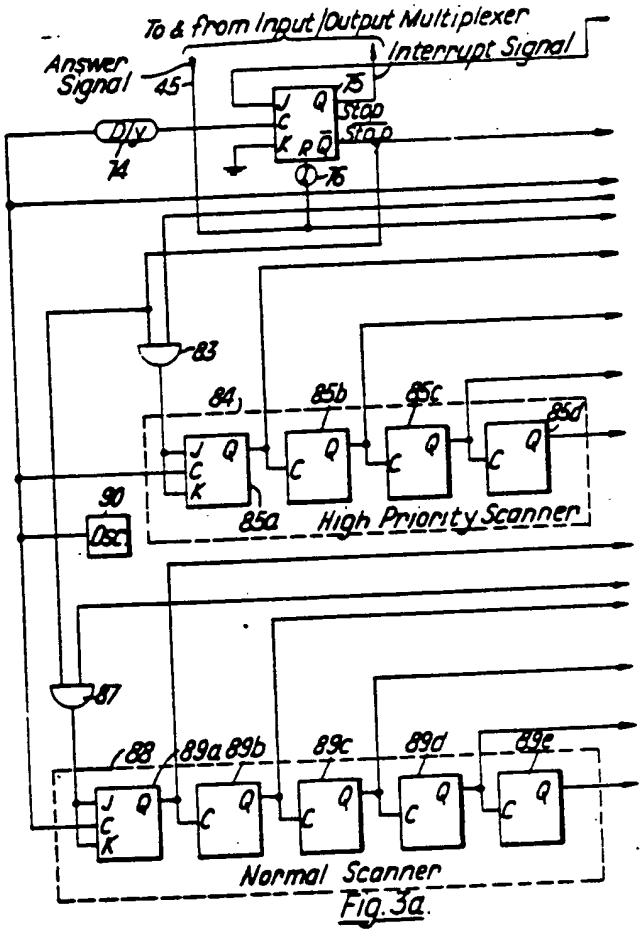


Fig.3a.

1359662 COMPLETE SPECIFICATION
9 SHEETS This drawing is a reproduction of the Original on a reduced scale
Sheet 5

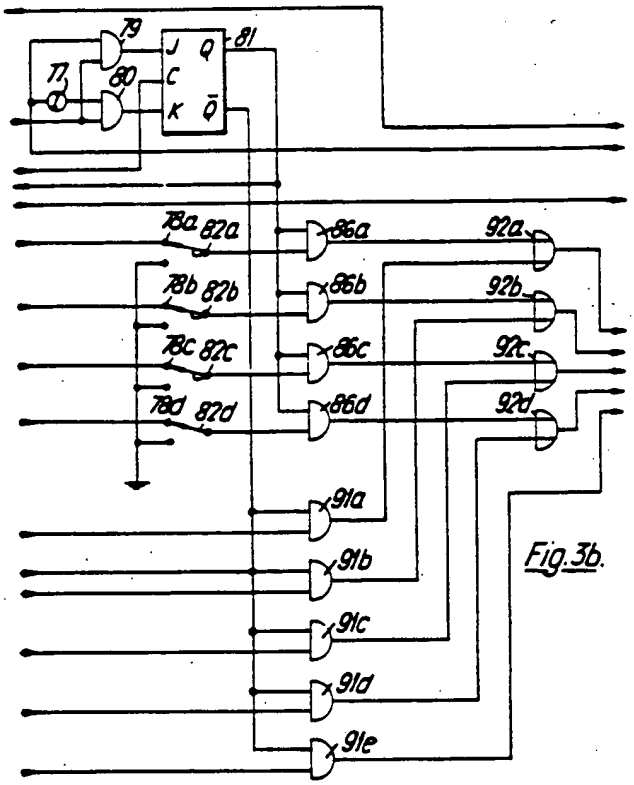


Fig.3b.

Fig.3a.	Fig.3b.	Fig.3c.

Fig.3d.

1359662 COMPLETE SPECIFICATION
9 SHEETS This drawing is a reproduction of the Original on a reduced scale
Sheet 6

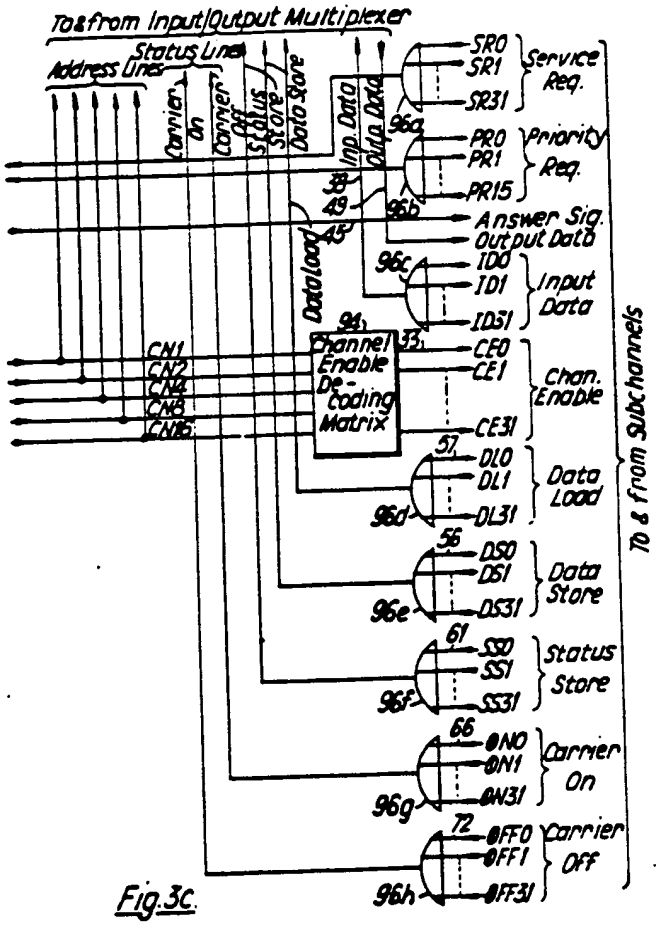


Fig.3c.

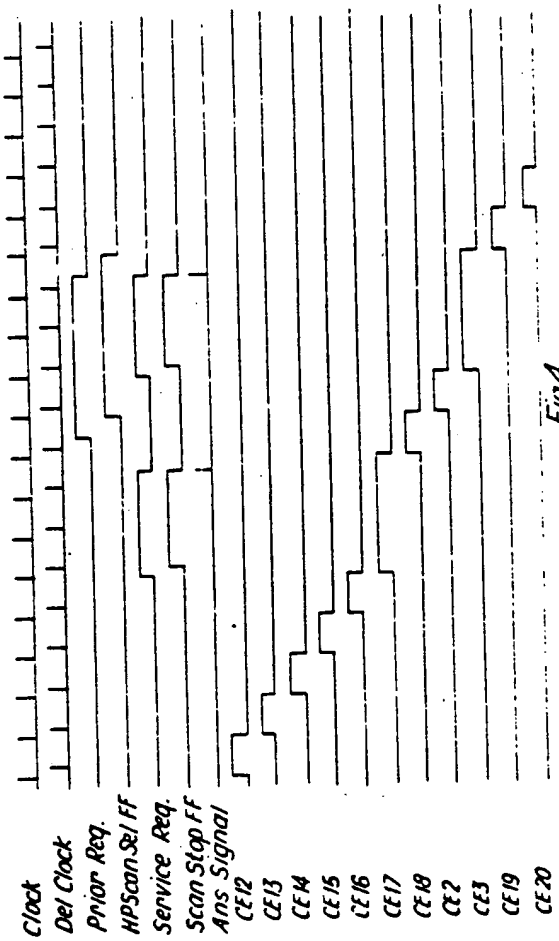

Clock
Del Clock
Prior Req.
HPScan Sel FF
Service Req.
Scan Stop FF
Ans Signal
CE12
CE13
CE14
CE15
CE16
CE17
CE18
CE2
CE3
CE19
CE20

Fig.4.

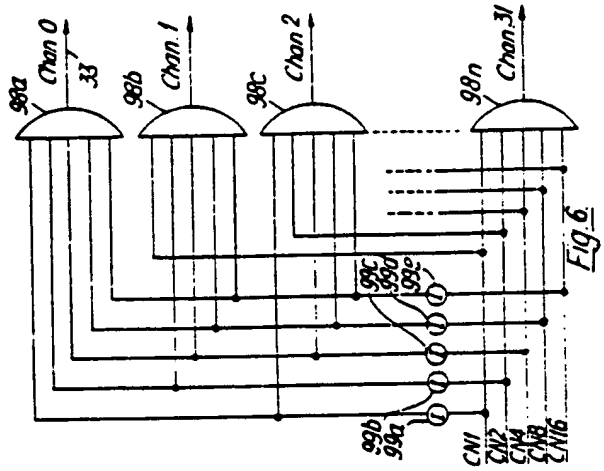

98a
Chan 0
33
98b
Chan 1
98c
Chan 2
98n
Chan 31
99c
99d
99e
99b
99a
CN1
CN2
CN4
CN8
CN16

Fig 6

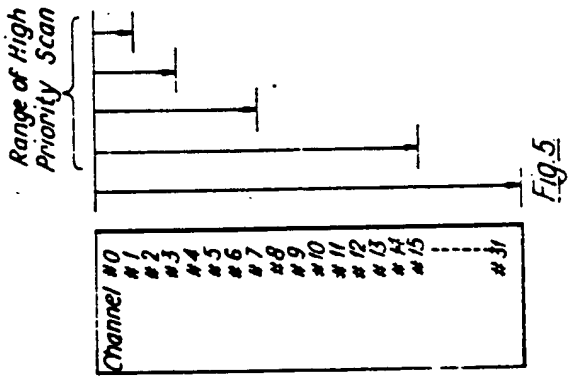

Range of High Priority Scan
Channel #0
#1
#2
#3
#4
#5
#6
#7
#8
#9
#10
#11
#12
#13
#14
#15
#31

Fig 5

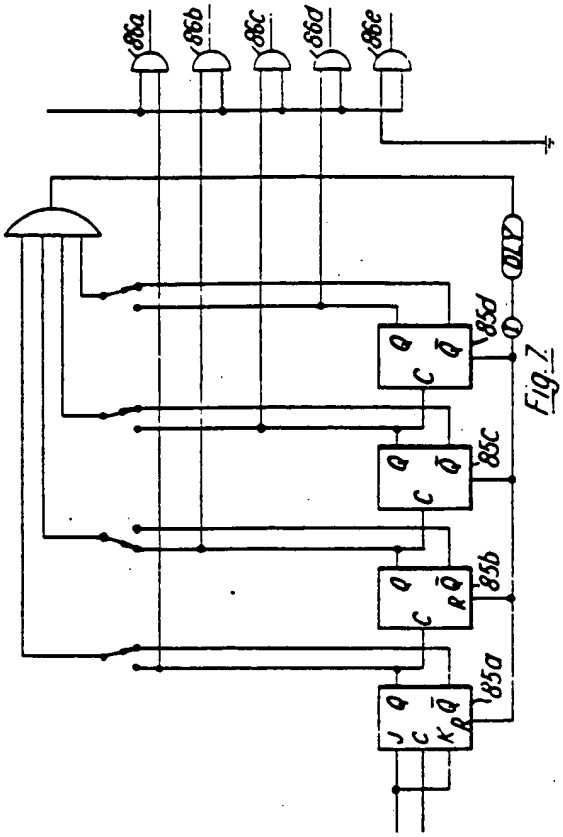


Fig.7